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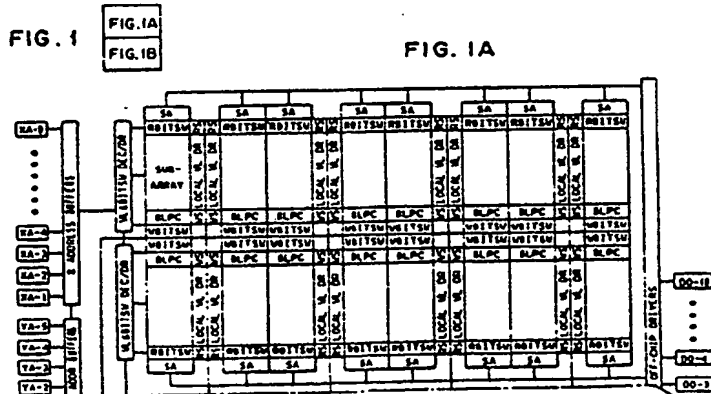
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54 **Pipelined memory chip.**

57 A semiconductor random access memory chip wherein the cycle time is less than the access time for any combination of read or write sequence. The semiconductor random access memory chip is partitioned into relatively small sub-arrays with local decoding (RS, WS) and precharging (BLPC). The memory chip operates in a pipelined manner with more than one access propagating through the chip at any given time and wherein the cycle time is limited by sub-array cycles wherein the cycle time is less than the access time for a memory chip having cycle times greater than access times for accesses through the same sub-array. The memory chip also incorporates dynamic storage techniques for achieving very fast access and precharge times.

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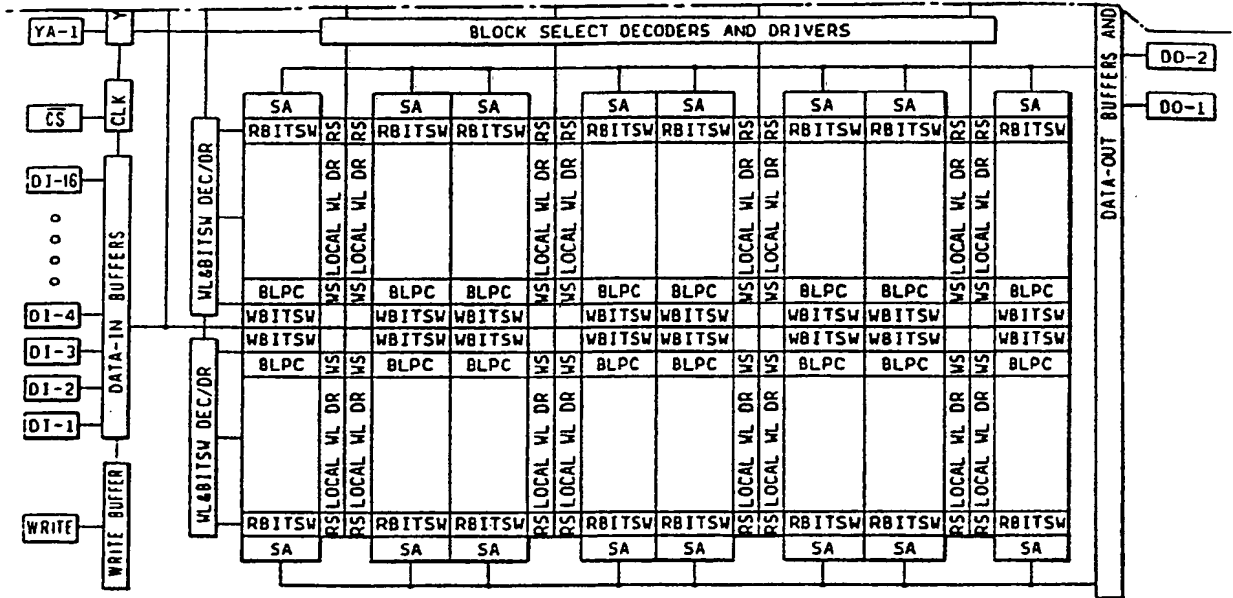


FIG. 1B

PIPELINED MEMORY CHIP

The present invention relates to semiconductor static and dynamic memories and more particularly, to pipelined semiconductor memories according to the preamble of claim 1.

The present invention includes a number of particular techniques and structures which are related to general concepts found in the prior art. For example, the present invention employs a form of sub-array structure, uses multiplexed sense amplifiers and incorporates a precharge technique.

Representative prior art references which describe memories with sub-arrays, but not for pipelined operation, include

U.S. Patent 4,569,036, issued February 4, 1986 to Fujii et al, entitled SEMICONDUCTOR DYNAMIC MEMORY DEVICE;

U.S. Patent 4,554,646, issued November 19, 1985 to Yoshimoto et al, entitled SEMICONDUCTOR MEMORY DEVICE;

U.S. Patent 4,542,486, issued September 17, 1985 to Anami et al, entitled SEMICONDUCTOR MEMORY DEVICE;

U.S. Patent 4,482,984, issued November 13, 1984 to Oritani, entitled STATIC TYPE SEMICONDUCTOR MEMORY DEVICE;

U.S. Patent 4,447,895, issued May 8, 1984 to Asano et al, entitled SEMICONDUCTOR MEMORY DEVICE;

U.S. Patent 4,384,347, issued May 17, 1983 to Nakano, entitled SEMICONDUCTOR MEMORY DEVICE;

U.S. Patent 4,222,112, issued September 9, 1980 to Clemons et al, entitled DYNAMIC RAM ORGANIZATION FOR REDUCING PEAK CURRENT.

References in the prior art directed to multiplexed sense amplifier input techniques include

U.S. Patent 4,511,997, issued April 16, 1985 to Nozaki et al, entitled SEMICONDUCTOR MEMORY DEVICE;

U.S. Patent 4,509,148, issued April 2, 1985 to Asano et al, entitled SEMICONDUCTOR MEMORY DEVICE;

U.S. Patent 4,477,739, issued October 16, 1984 to Proebsting et al, entitled MOSFET RANDOM ACCESS MEMORY CHIP;

U.S. Patent 4,447,893, issued May 8, 1984 to Murakami, entitled SEMICONDUCTOR READ ONLY MEMORY DEVICE;

U.S. Patent 4,410,964, issued October 18, 1983 to Nordling et al, entitled MEMORY DEVICE HAVING A PLURALITY OF OUTPUT PORTS.

Descriptions of techniques using precharge signals dependent upon a memory address are found in U.S. Patent 4,520,465, issued May 28, 1985 to Sood, entitled METHOD AND APPARATUS FOR SELECTIVELY PRECHARGING COLUMN LINES OF A MEMORY and U.S. Patent 4,513,372, issued April 23, 1985 to Ziegler et al, entitled UNIVERSAL MEMORY.

"A 32b VLSI System", Joseph W. Beyers, et al, 1982, Digest of Technical Papers, 1982, IEEE International Solid-State Circuits Conference, pages 128-129; mentions that a 128 Kb RAM is pipelined.

The object of the present invention is to provide a semiconductor random access memory chip grouped into a plurality of sub-arrays wherein the cycle time is less than the access time for any combination of read or write sequence.

Still another object of the present invention is to provide a semiconductor random access memory chip including relatively small memory sub-arrays which are operated in a pipelined manner with more than one access propagating through the chip at any given time and wherein the cycle time is limited by sub-array cycles.

The solution of the objects is described in the characterizing part of claim 1.

Further solutions are described in the other claims.

Brief Description Of The Drawings

FIG. 1 is a schematic illustration of a 256K semiconductor memory chip partitioned into a plurality of sub-arrays including bitswitches, sense amplifiers, word line drivers and precharge circuits according to the principles of the present invention.

FIG. 2 is a schematic illustration of a simplified depiction of a conventional 64K semiconductor memory chip including a plurality of macros according to the prior art.

FIG. 3-1 is a schematic illustration of a simplified depiction of a semiconductor memory chip including both a local precharge/reset technique and block address circuitry according to the principles of the present invention.

FIG. 3-2 is a schematic illustration of a simplified depiction of a semiconductor memory chip similar to that of FIG. 3-1 including both a local precharge reset technique and block address compare circuitry and further including a compare technique according to the principles of the present invention.

FIGS. 4 and 5 are illustrations of timing diagrams useful in describing the operation of the semiconductor memory structure of the present invention.

FIGS. 6 and 7 are block diagram illustrations of the pipeline segments in the access path of a semiconductor memory chip according to the principles of the present invention.

Referring to FIG. 1, a schematic illustration, referred to in the art as a floor plan, is shown for a 256K bit embodiment of a CMOS semiconductor chip for a cache memory according to the present invention.

The particular embodiment of the 256K bit chip shown in FIG. 1 uses a second level metal layer to partition the chip into thirty-two 8K bit sub-arrays. Each sub-array is organized as 128 word lines by 64 bitline pairs with 4-way bitswitches and 16 resistively decoupled, self-timed sense amplifiers which are located inboard, next to the sub-array because of the use of a second level metal layer. The structure uses standard CMOS memory cells composed of six devices. The present invention may include, however, embodiments using single layer metal as well as three, four or more metal layers.

More specifically, the 256K bit chip structure of FIG. 1 includes 32 sub-arrays arranged in 8 columns and 4 rows. The abbreviations used in FIG. 1 refer to the following elements.

	CS	Chip Select Not Input	
	SA	Sense Amplifier	
	BITSW	Bitswitch	
	RBITSW	Read Bitswitch	
	WBITSW	Write Bitswitch	
	RS	Local Read BitSwitch	
		Decoder/Driver	
	WL	WS	Local Write BitSwitch
		Decoder/Driver	Word Line
	BL	WLDR	Word Line Driver
		BLPC	Bitline Precharge
		DEC	Decoder
		DR	Driver

... table continued ...

	ADDR AMPS	Address Amplifiers
	DI	Data In
	DO	Data Out
	XA	X-Address Input
	YA	Y-Address Input

As shown in FIG. 1, each sub-array includes a separate read bitswitch, write bitswitch, bitline precharge circuit, local word line driver and sense amplifier. Local word line and local read and write bitswitch decoder/drivers are associated with each of the 32 sub-arrays. X address amplifiers and Y address amplifiers are coupled to the word line and bitswitch decoder/drivers and block select decoder/drivers respectively, under control of a clock signal generated from the Chip Select Not Input. Data-in amplifiers provide inputs to each of the 32 sub-arrays under control of the clock signal and the write input.

The sense amplifiers associated with each of the 32 sub-arrays are connected to data output lines via data-out latches and off-chip drivers.

The sub-array arrangement illustrated in the embodiment of FIG. 1 includes local decoding and

precharging and therefore, is operable in a pipelined manner with more than one access being capable of propagating through the chip at any given time. The cycle time of the chip is limited by the sub-array cycle time.

Features of the chip of FIG. 1 include a chip cycle time that is less than the access time, while also having a fast access time. This is accomplished by a number of techniques.

One technique employed in FIG. 1 is that blocks in a critical path are designed such that their active plus precharge time is less than the access time of the chip. A key feature of the invention is that dynamic storage techniques are used to make it possible to achieve very fast access and precharge times. Also, self-timing is used block-to-block and internally.

To reduce word line delay, the chip of FIG. 1 is segmented into 8 local word lines with the global word lines on a first level metal layer and the local word lines on a polycide layer.

The delay in developing data signals on the bitlines is reduced by segmenting the chip into 4 rows and by wiring the bitlines on a second level metal layer.

The block select decoders and driver circuits are centered to reduce metal RC delays.

Separate read and write paths are used with the write bitswitches placed at the opposite ends of the bitlines from the read bitswitches to minimize delay for both a read and write operation.

The 256K SRAM bit chip using the floor plan of FIG. 1 with sub-arrays is operated in a pipelined manner with more than one access propagating through the chip at any given time. In addition, the floor plan with inboard sense amplifiers is applicable to DRAM operation with only a slight increase in access time with the restore portion of the cycle being hidden by the pipelined mode of operation.

As previously stated, in the floor plan for a 256K SRAM shown in FIG. 1, the chip has been partitioned into 32 128 WL x 64 BL sub-arrays by making use of second layer metal. The optimum size and number of sub-arrays is influenced by chip access time requirements and array utilization. The second level of metal also makes it practical to have inboard sense amplifiers for improvement of access time by reducing the loading on the output lines. Bitswitches are used so a sense amplifier can be shared between four bit lines, reducing the loading on the sense-amp set signal, compared to having a sense-amp for each bitline. The sense amplifiers for each sub-array are self-timed locally and totally self-contained.

Each of the sub-arrays in the new floor plan is essentially self contained, with its own localized word line driver, self-timed sense amplifier circuitry and precharge circuitry. During an access only a single sub-array is activated. Having only a small fraction of the chip (1/32 for the 256K example) accessed each cycle has important ramifications for the design of a pipelined memory with more than one access propagating through the chip at a given time.

In simplified form, a prior art memory chip consists of a number of blocks or macros as shown in FIG. 2. During an access, data simply ripples from block to block with one block activating the next one and a global reset is used.

To achieve cycle time less than access time so the RAM can be pipelined, a localized precharge is performed as shown in FIG. 3-1 as an improvement over prior art global precharge as employed in FIG. 2. With the subdivided floor plan, the precharge signal can be generated locally and the loading on the precharge clock line is not large. The 256K design has only 8K bits of sub-array which must be precharged each cycle. The sub-arrays can be considered as an array of chips with only one of them being activated each selection. The sub-arrays with their own localized word line drivers, bitswitches, self timed sense amplifiers and precharge circuits are virtually independent chips.

Additionally, each of the global blocks, external to the sub-array local circuitry, has self-timed precharge and reset circuitry. In other words, each block in the critical path shown in FIG. 3-1 is switched into the active state by the previous blocks input signal, but is returned to its precharge/standby state by self-contained circuitry.

Being able to precharge a block very quickly after it has performed its function in anticipation of the next access is a key requirement for a memory with cycle time less than access time. The minimum time before another access can be started is the active time plus the precharge time for the slowest block in the access path. The sub-array precharge, because of the need to accurately equalize the bit lines, is difficult to accomplish in a short period of time. Thus, the chip cycle time is limited by the sub-array cycle time. A six-device CMOS cell, as used in the 256K SRAM, allows the shortest cycle time.

The floor plan of FIG. 1 with inboard sense amplifiers makes it possible to achieve almost the same access time for a Dynamic Random Access Memory (DRAM) array as an SRAM array. However, because of the need to restore the data in the accessed cell, it will take considerably longer for the precharge portion of the cycle.

In order to operate the chip of FIG. 1 in a pipelined mode of operation for the cases where a long precharge is needed, initiation of another access to the chip is permitted as long as that access is not to the

same sub-array as in the last three previous accesses. As shown in FIG. 3-2, this is accomplished by comparing the sub-array selection bits with those of the previous three accesses. If the previous accesses are to different sub-arrays resulting in a no match with the compare function, the new access would proceed. For the case where the compare found a match, the chip would go into a wait state until the sub-array precharge is completed and the new access is initiated.

By storing data from sequential addresses in different sub-arrays, it is possible to minimize the probability of an access to the last three accessed sub-arrays. For the 256K example given, there are 32 sub-arrays. Unless addresses were incremented by 1/2 word (32) increments the probability of returning on successive accesses to the last three sub-arrays accessed is small. For random accesses, the probability of accessing one of the last three sub-arrays accessed is 3/32. A compare on five of the address bits is required each access. Thus, it is possible for a memory chip with long sub-array precharge to operate in a pipelined mode the majority of the time with cycle time less than access time.

The systems implication of a pipelined memory with cycle time less than access time can be understood by considering the timing diagram of FIG. 4 and FIG. 5 and the pipeline segment block diagrams of FIG. 6 and FIG. 7. Two cases are considered. The first in FIG. 4 and FIG. 6, assumes that the active plus precharge times of each block is less than 1/2 the access time. Therefore, the chip can be pipelined with a cycle time of 1/2 the access time for both a read and a write. No comparisons are needed on incoming addresses. For this case the bandwidth of the chip is twice what it would be for a chip with access time = cycle time that is not pipelined.

The second case (FIG. 5 and FIG. 7) assumes that the active plus precharge time of the slowest block (the sub-array) is twice the access time and that all other blocks are less than 1/2 the access time. It is also assumed that comparisons are done on incoming address to check whether or not the access is to a sub-array accessed on one of the last three cycles. For the case where the access is not to one of these same sub-arrays and there is no match on the compare, the chip will run in a pipelined mode with a cycle time of 1/2 the access time. If the access is to one of these same sub-arrays, there will be a match on the incoming address and the cycle time will be extended. Therefore, the bandwidth for this pipelined case compared to a chip that is not pipelined but has the same access time and a cycle time of twice the access time is

$$BW \approx BW_0 \left(1 + \left(\frac{TNA - AC}{TNA} \right) \times 3 \right) \quad (1)$$

where

BW_0 = band width without pipelining

BW = band width with pipelining

TNA = total number of accesses

AC = accesses with compare.

If the accesses are random in nature, the bandwidth can be given by

$$BW \approx BW_0 \left(1 + \left(1 - P_c \right) \times 3 \right) \quad (2)$$

$$BW \approx BW_0 \left(1 + \left(\frac{NSA - 3}{NSA} \right) \times 3 \right) \quad (3)$$

where

P_c = probability of a compare

NSA = number of sub-arrays.

Thus for either random or sequential addresses one should see almost a four times increase in bandwidth compared to a conventional chip. For a DRAM, the amount of time a chip is not available because of refreshing would be reduced by this same factor.

Thus, two approaches to the design of a pipelined memory chip with cycle time less than access time using a floor plan with sub-arrays have been described. The first approach assumes the active plus

precharge portions of each block is less than the access time. In the second approach, it is assumed that the active plus precharge portions of the sub-array block is greater than the access time, and that the active plus precharge portions of the rest of the blocks is less than the access time. For both cases, a substantial increase in memory chip bandwidth is possible in memory systems using SRAM and DRAM chips.

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Claims

1. Pipelined semiconductor 2^n Kbit memory chip, n being an integer not less than 2, said chip being segmented into a plurality of 2^{n-y} memory sub-arrays of 2^y Kbits arranged in columns and rows on said chip, characterized in that each one of said 2^{n-y} memory sub-arrays includes a separate associated word line driver circuit means, sense amplifier circuit means and independent precharge circuit means connected thereto.
2. Pipelined semiconductor 2^n Kbit memory chip according to claim 1, characterized by a plurality of word lines, a first group of said plurality of word lines disposed on a first metal layer and a second group of the plurality of word lines disposed on a second metal layer, and a plurality of bit lines disposed on the second metal layer.
3. Pipelined semiconductor 2^n Kbit memory chip according to claim 1, characterized in that each of said independent precharge circuit means of each of said segmented memory sub-arrays provides local self-timed reset and precharge function for each segmented memory array independent of said other of said plurality of 2^{n-y} memory arrays.
4. Pipelined semiconductor 2^n Kbit memory chip according to claim 3, characterized in that each of the segmented memory sub-arrays further includes a separate read bitswitch and read switch circuit means and a separate write bitswitch and write switch circuit means, and wherein a separate word line and bitswitch decoder/driver circuit means is connected to the said memory sub-arrays in each of said rows on said chip.
5. Pipelined semiconductor 2^n Kbit memory chip according to claim 3, characterized in that the memory chip exhibits an access time t for providing data from said memory chip and wherein said local reset and precharge circuits of each of said segmented memory sub-arrays provides a cycle time for each sub-array which is less than chip access time t .
6. Pipelined semiconductor 2^n Kbit memory chip according to claim 5, characterized in that the segmented memory sub-arrays including independent local decoding and precharging means operate in a pipelined manner with greater than one access propagating through said 2^n Kbit memory chip at one time.
7. Pipelined semiconductor 2^n Kbit memory chip according to claim 6, characterized by further including row and column address circuits disposed on said chip connected to said word line and bitswitch decoder/driver circuit means and responsive to input address access signals for selecting ones of said 2^{n-y} segmented memory sub-arrays for access.
8. Pipelined semiconductor 2^n Kbit memory chip according to claim 3, characterized by comparing circuits for determining said sub-arrays being accessed by separate access signals.
9. Pipelined semiconductor 2^n Kbit memory chip according to claim 3, characterized in that the memory chip exhibits an access time t , further including global blocks on said chip external to said sub-arrays each containing clock circuit means, address buffer means, row decoder means, data output bluffer means and word driver means associated with said plurality of sub-arrays, each of said global blocks including separate reset and precharge circuit means for providing a cycle time for each of said global blocks which is less than chip access time t .

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FIG. 1A
FIG. 1B

FIG. 1

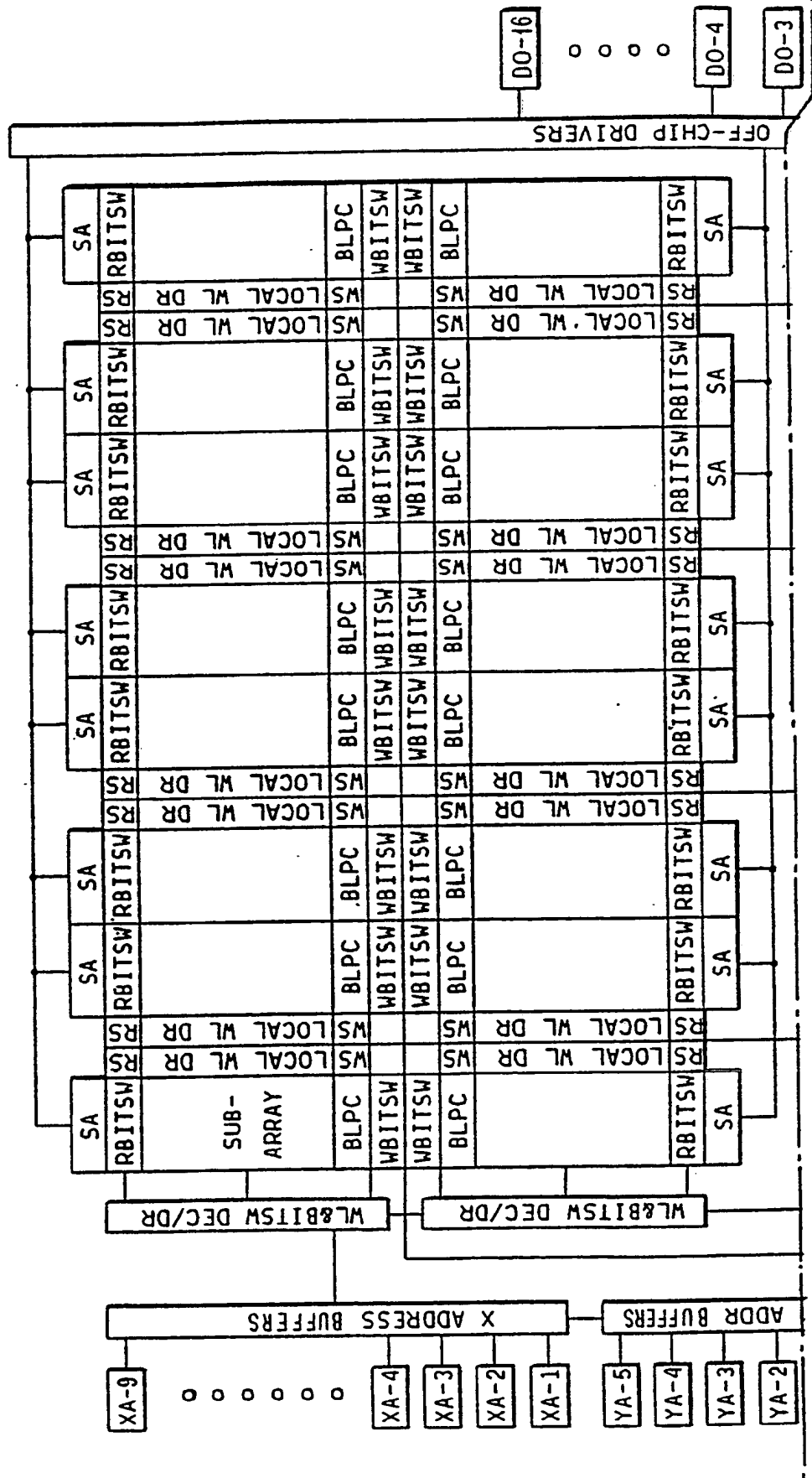


FIG. 1A

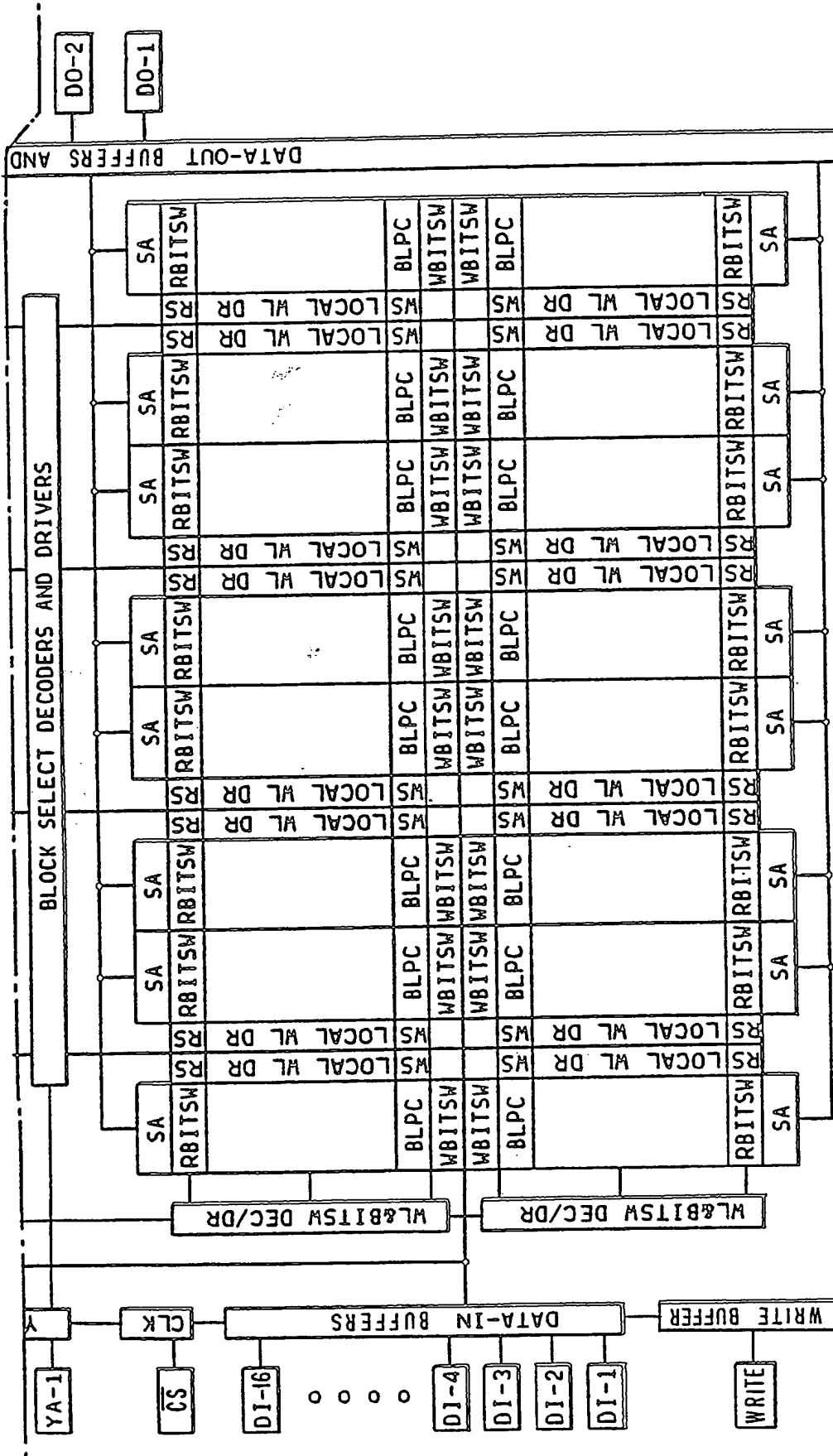


FIG. 1B

FIG.2

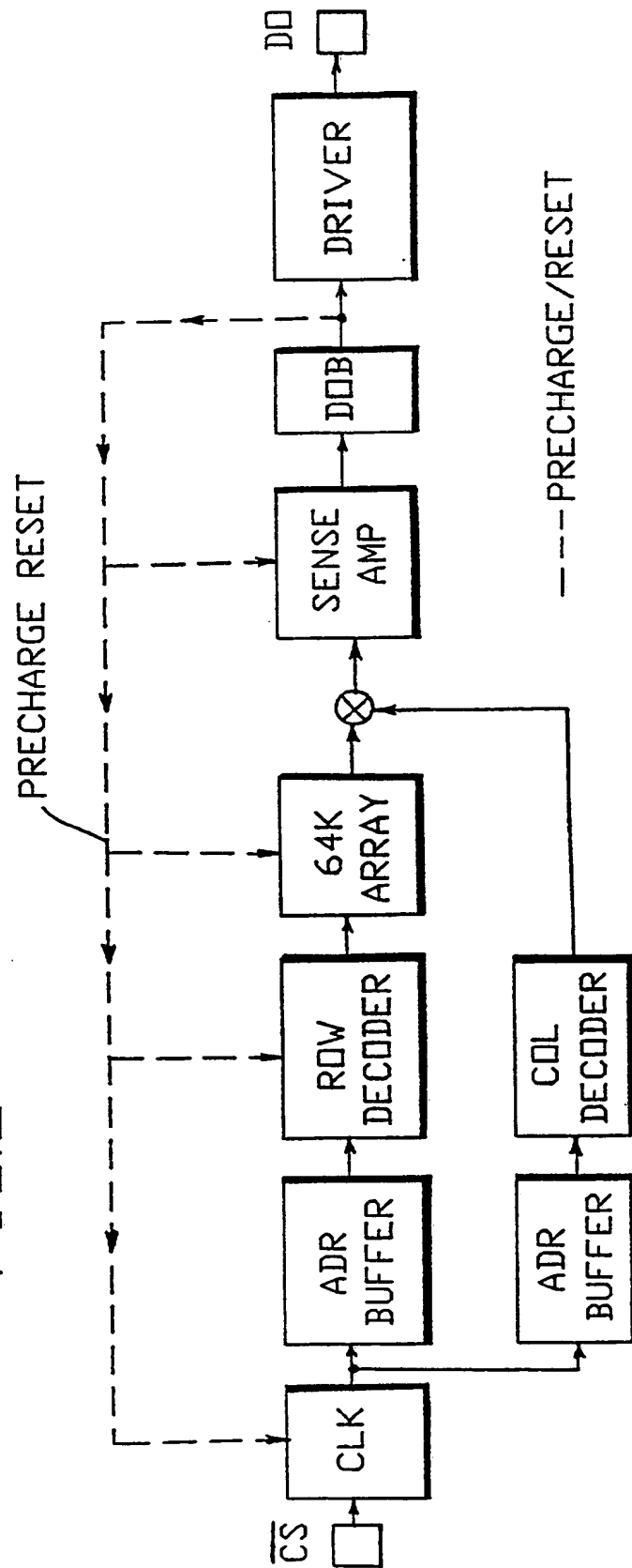


FIG. 3-1

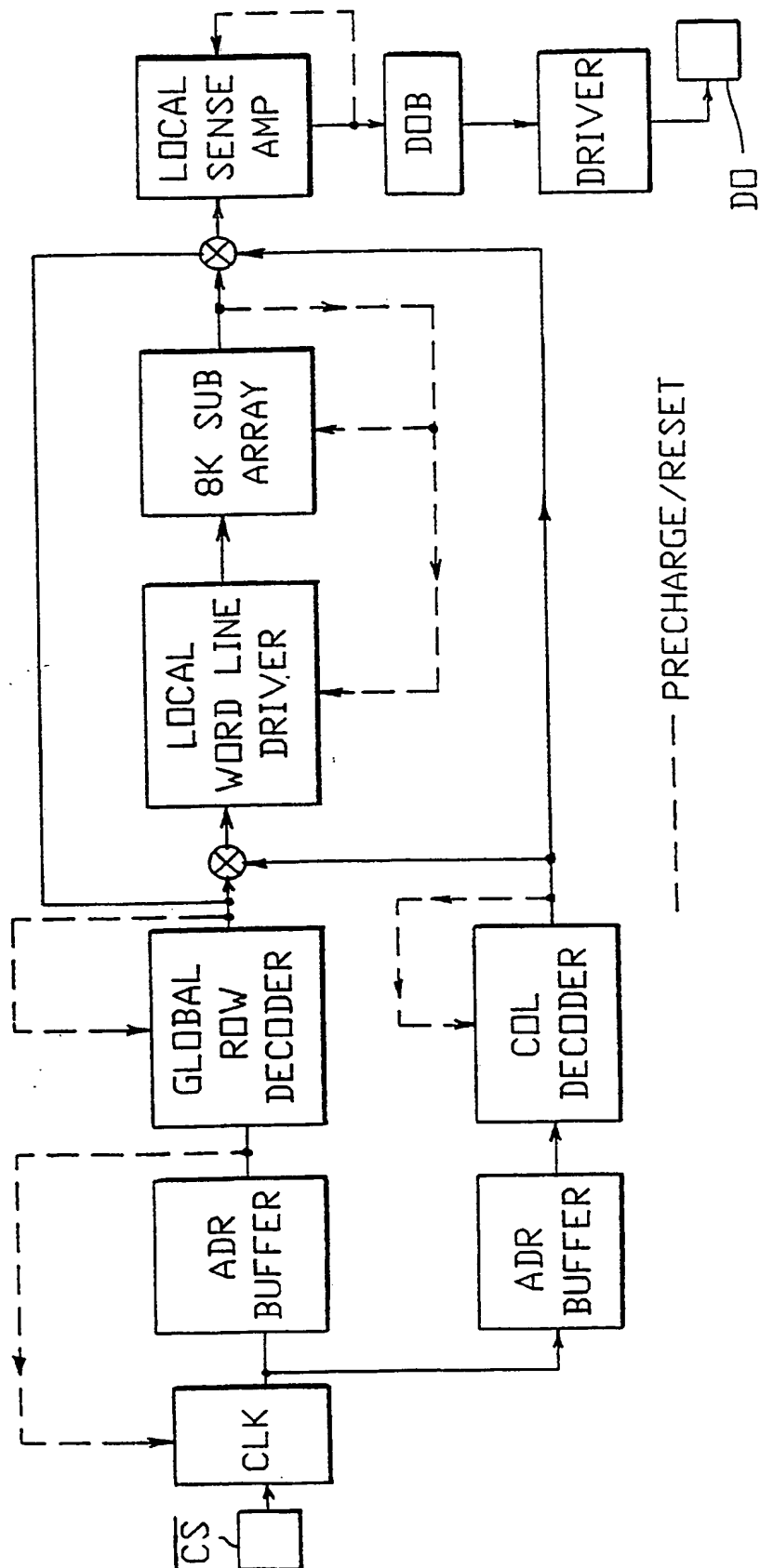


FIG. 3-2

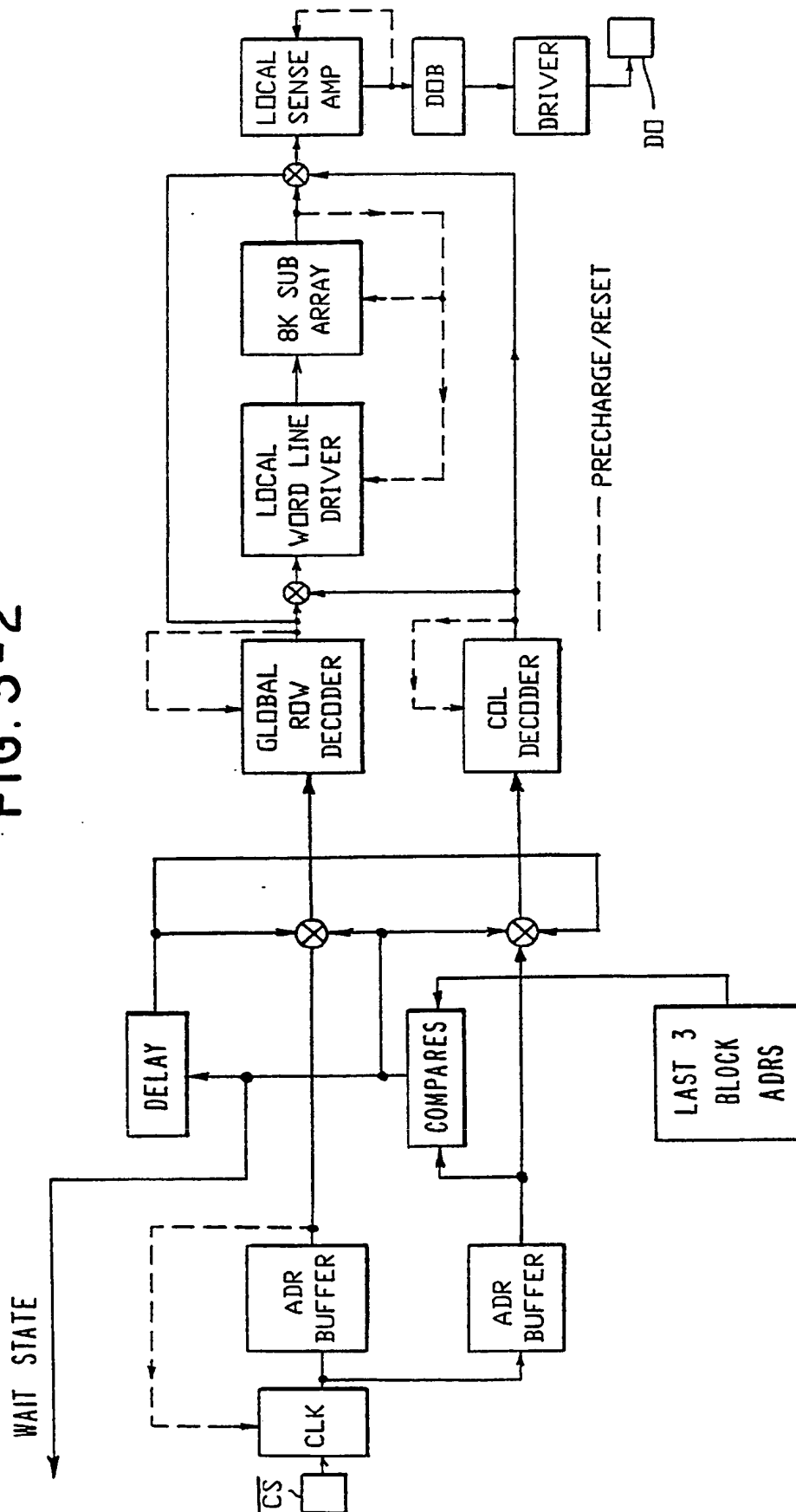


FIG.4
PIPELINED MEMORY CHIP

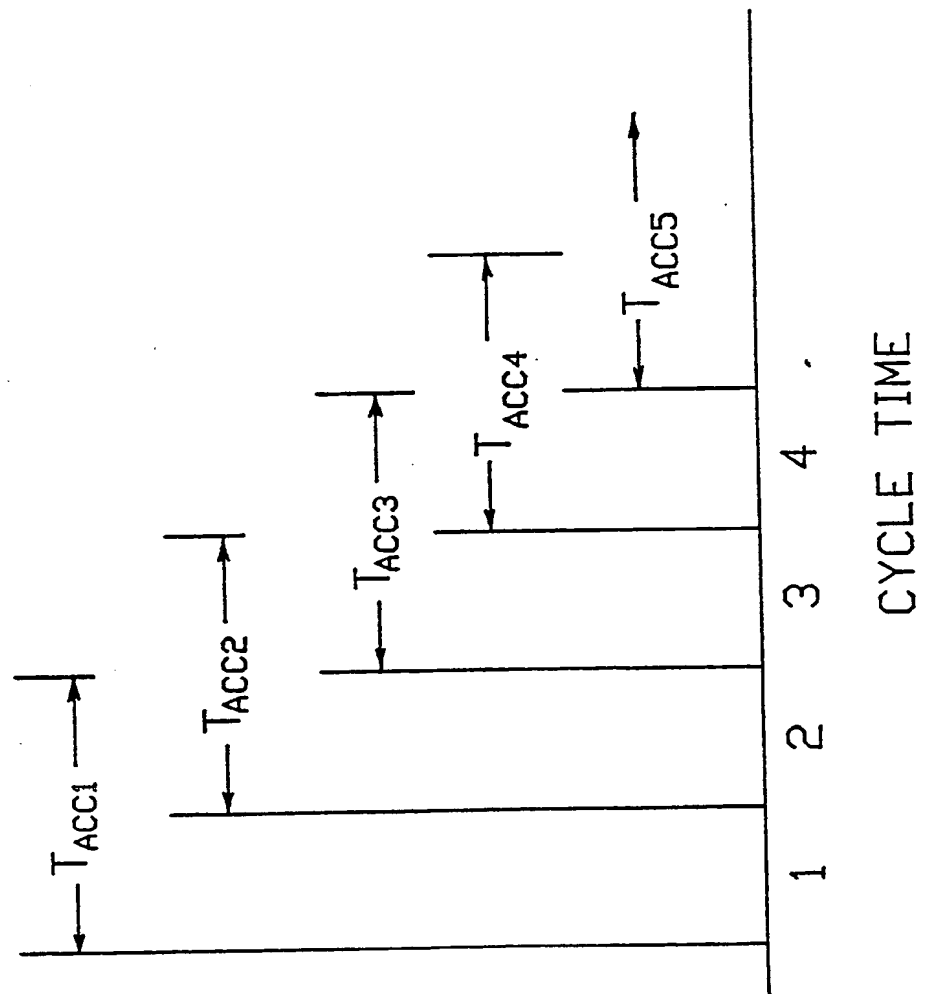


FIG. 5 a,b,c,d,N - BLOCK ADDRESSES

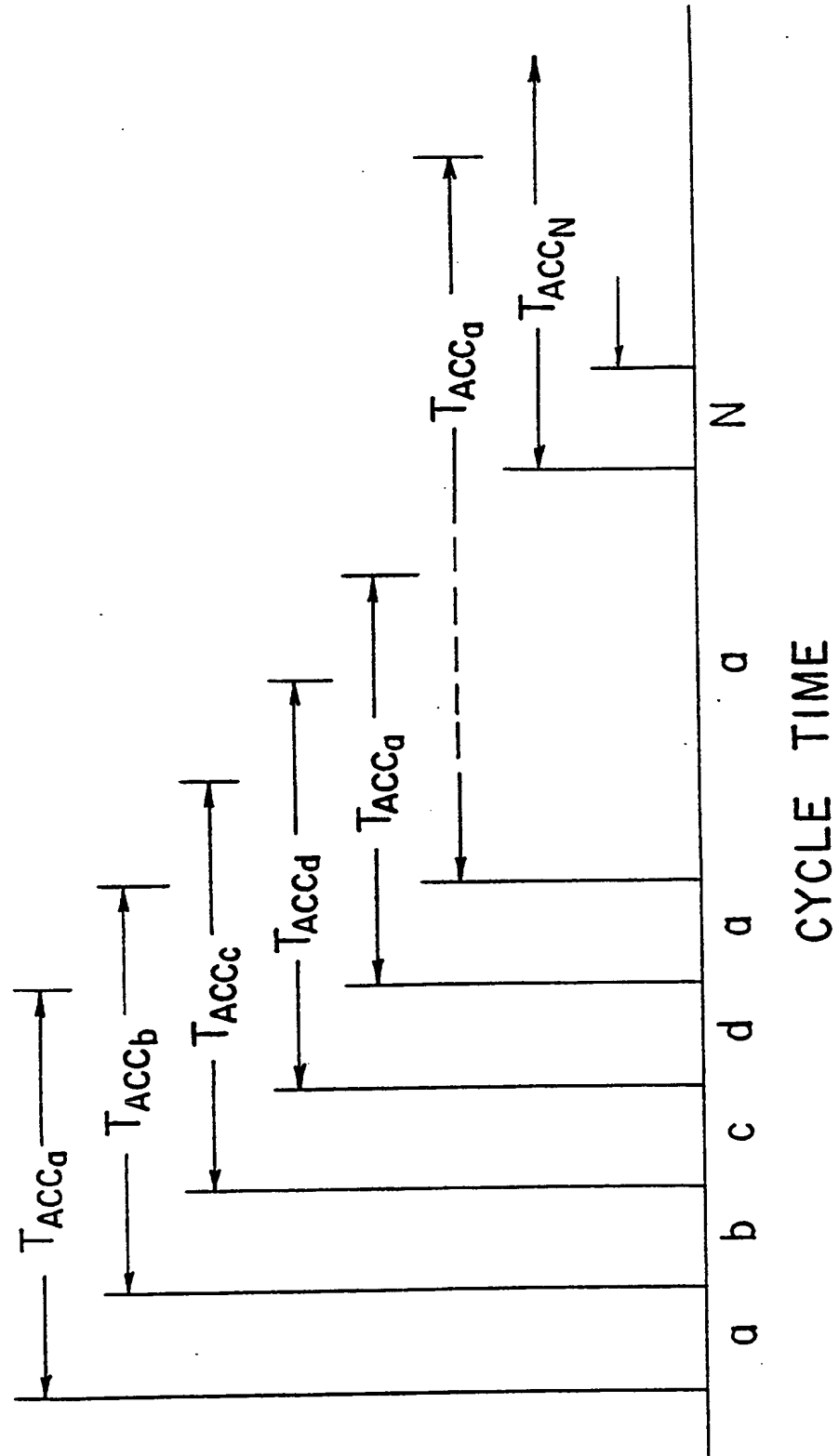
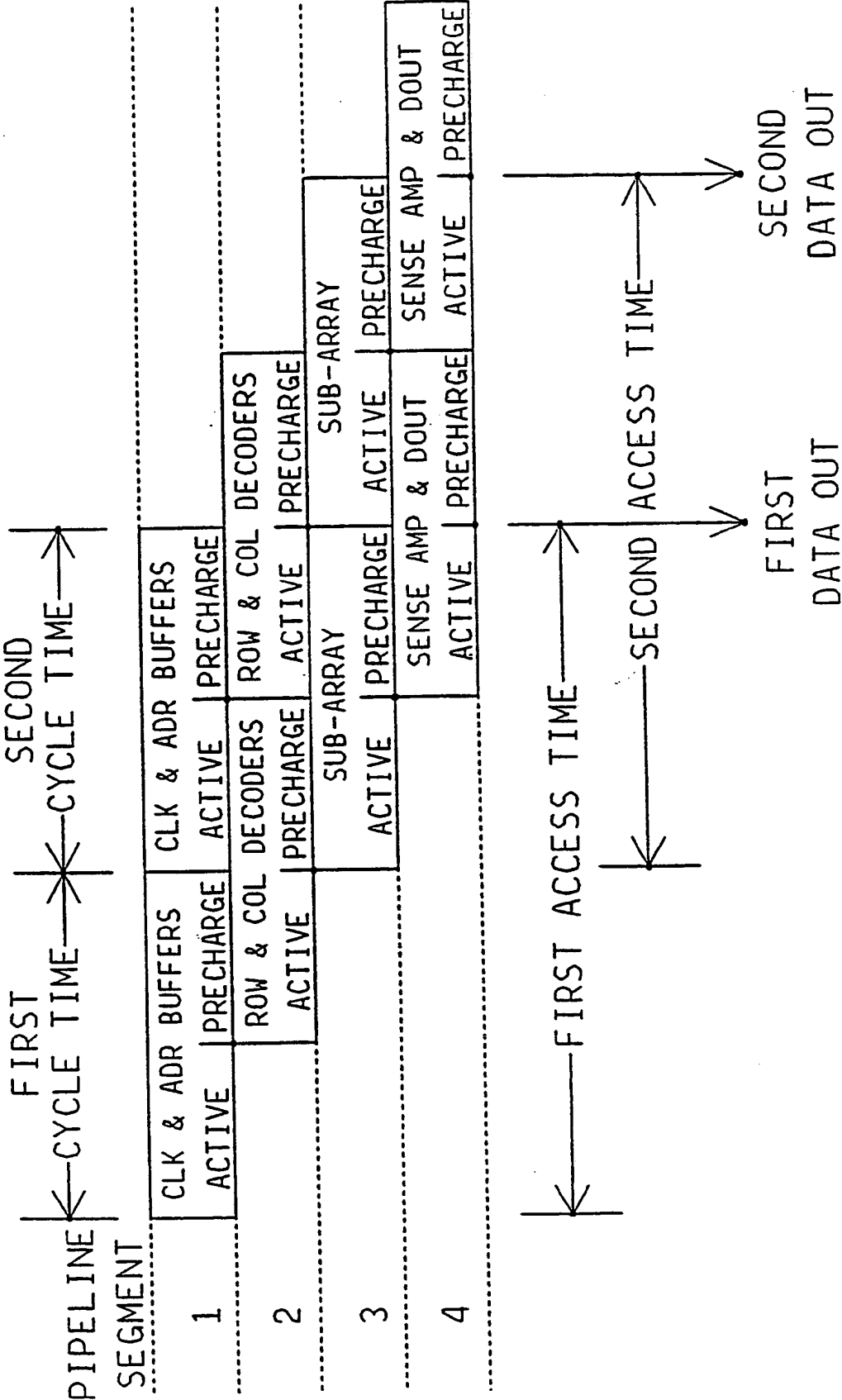


FIG. 6



BLOCK BLOCK BLOCK BLOCK
ADR=A ADR=B ADR=C ADR=D ADR=A

FIG. 7A

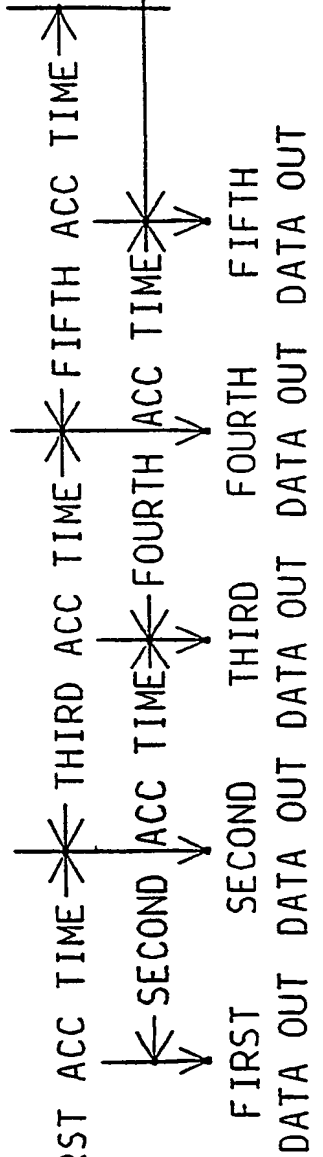
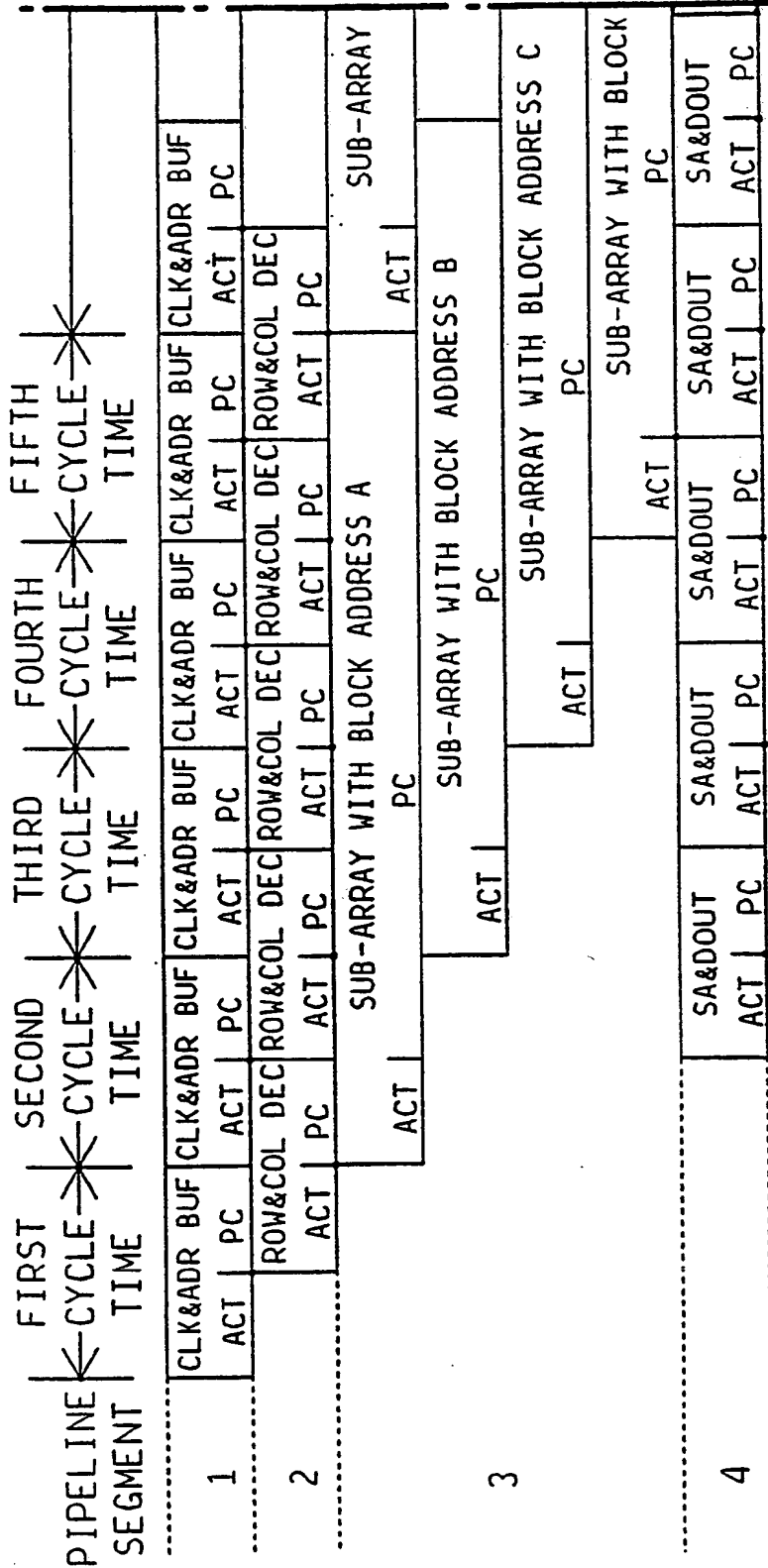
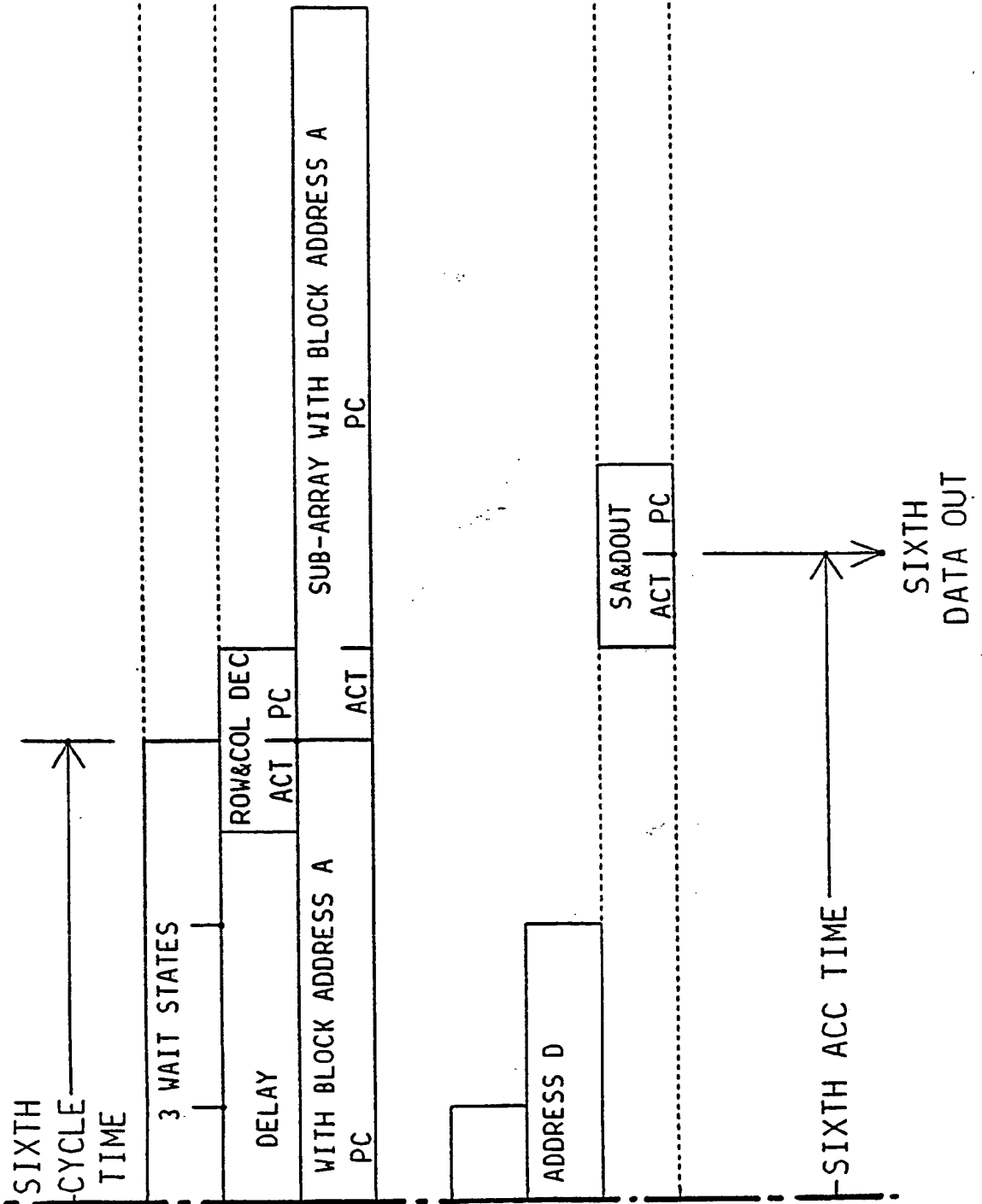


FIG. 7

FIG. 7A FIG. 7B

FIG. 7B

BLOCK
ADR=A





DOCUMENTS CONSIDERED TO BE RELEVANT			EP 88110694.2
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	US - A - 4 597 061 (CLINE et al.) * Abstract; column 1, line 33 - column 2, line 4; column 4, line 26 - column 6, line 63; fig. 1 *	1	G 11 C 8/00 G 11 C 11/40 G 11 C 7/00
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A	EP - A2 - O 199 134 (INTERNATIONAL BUSINNES MACHINES) * Abstract; column 1, line 41 - column 2, line 21; column 6, line 1 - column 7, line 43; fig. 5,6 *	1	
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D,A	1982 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, DIGEST OF TECHNICAL PAPERS, February 1982, Coral Gables, US J.W.BEYERS "A 32b VLSI System" pages 128,129 * Page 128, table 1 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.4) G 11 C
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D,A	US - A - 4 569 036 (FUJII et al.) * Abstract; column 1, lines 5-65; column 4, lines 28-53; column 5, lines 16-40; fig. 1,2,5 *	1,6,7	
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A	EP - A2 - O 145 488 (FUJITSU) * Page 1, line 18 - page 2, line 20; page 2, line 33 - page 3, line 27; fig. 1 *	1,6,7	
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The present search report has been drawn up for all claims			
Place of search VIENNA		Date of completion of the search 30-11-1988	Examiner HAJOS
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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
D, A	US - A - 4 520 465 (S00D) * Abstract; lines 41-64; fig. 1 * -----	1, 6, 7	
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)
The present search report has been drawn up for all claims			
Place of search VIENNA		Date of completion of the search 30-11-1988	Examiner HAJOS
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